REMARKS

Claims 1, 2 and 4-22 are pending in this application. Claims 1, 7, 10, 21 and 22 are independent claims. By this supplemental amendment: claims 1, 4, 7-9 and 22 are amended, and claim 3 is expressly canceled. Reconsideration in view of the above supplemental amendments and following amended remarks is respectfully solicited.

I. THE CLAIMS DEFINE PATENTABLE SUBJECT MATTER

The Office Action rejects claims 1 and 2 under 35 U.S.C. §102(e)as being anticipated by Applicants' Prior Art Figure 19 and the Admitted Prior Art in the disclosure of page 5. This rejection is respectfully traversed.

Applicants respectfully submit that cited Figure 19 and the admitted prior art in the disclosure of page 5 of applicants' specification fails to teach or suggest each and every feature as set forth in the claimed invention.

In a semiconductor device of the claimed invention, particularly claims 1 and 7, the electrical properties of the semiconductor element changes so that the element fails to operate properly when the semiconductor element becomes unleveled. Thus, in this configuration it is possible to protect the semiconductor element from any type of circuit analysis once detached or unleveled, and hence secrets can be concealed.

Moreover, the claimed configuration is arranged such that when the semiconductor element is subjected to processing, a stress is applied to the semiconductor elements because of the processing. Due to this predetermined stress, at least part of the semiconductor element is deformed when the element is removed from the board. Thus, the leakage of secrets from the semiconductor

design (unmounted element) once detached from the board can be prevented due to the deformity of the semiconductor element.

In contrast, in the admitted prior art on page 5 of applicants' specification, at least a part of the back of the semiconductor element is not subjected to processing, thus applying a predetermined stress to the semiconductor element due to the processing. As a result, the element does not deform when detached from the board. As such, in contrast to the present invention, it is very easy to carry out circuit analysis of the prior art element once the element is removed from the board.

According to MPEP §2131, "a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. Of California*, 814 F.2d 628, 631, 2 USPQ2d 1051 (Fed. Cir. 1987). "The identical invention must be shown in as complete detail as is contained in the …claims." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913 (Fed. Cir. 1989). The elements must be arranged as required by the claims, but this is not an *ipsissimis verbis* test, i.e., identity of terminology is not required. *In re Bond*, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990).

Applicants respectfully submit that the Office Action has failed to establish the required *prima facie* case of anticipation because the cited admitted prior art fails to teach or suggest each and every feature as set forth in the claimed invention.

Applicants respectfully submit that independent claims 1, 7, 21 and 22 are allowable over the admitted prior art for at least the reasons noted above.

As for each of the dependent claims not particularly discussed above, these claims are also allowable for at least the reasons set

forth above regarding their corresponding independent claims, and/or for the further features claimed therein.

Accordingly, withdrawal of the rejection of claims 1 and 2 under 35 U.S.C. §102(e) is respectfully solicited.

II. CONCLUSION

In view of the foregoing, Applicants respectfully submit that the application is in condition for allowance. Favorable reconsideration and prompt allowance are earnestly solicited.

Should the Examiner believe that anything further would be desirable to place this application in better condition for allowance, the Examiner is invited to contact Carolyn T. Baumgardner (Reg. No. 41,345) at (703) 205-8000 **to schedule a Personal Interview**.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment from or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §1.16 or under 37 C.F.R. §1.17; particularly, the extension of time fees.

Respectfully submitted,
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CG/CTB/mpe
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Attachment: Version with Markings to Show Changes Made

VERSION WITH MARKINGS SHOWING CHANGES MADE

IN THE CLAIMS:

The claims are amended as follows:

1. (Twice Amended) A semiconductor device, in which a semiconductor element with an integrated circuit is secured to a board,

wherein the semiconductor element is secured in a level position and specified to operate normally only when the semiconductor element is maintained in this level position,

wherein at least part of a back of the semiconductor element is subjected to processing and a stress is applied to the semiconductor element because of the processing [secured with such a stress level applied on a back thereof that when the semiconductor element is detached from the board], wherein at least part of the semiconductor element [at least partially deforms] is deformed when the semiconductor element is detached from the board, due to the stress.

4. (Twice Amended) The semiconductor device as defined in claim 1,

wherein the semiconductor element has a thickness of 50 μm or less in the area where the semiconductor element is processed [secured].

7. (Twice Amended) A method of manufacturing a semiconductor device, comprising,

securing a semiconductor element having an integrated circuit to a board so [as to be level with the board] that the semiconductor element is maintained in a level position,

[securing] subjecting at least a part of a back of the semiconductor element to processing, wherein the processing applies a stress to the semiconductor element [the board so as to develop a stress level that reacts when the semiconductor element is detached from the board,] causing at least a part of the semiconductor element to deform when removed from the board, wherein the semiconductor element operates normally only when the semiconductor device is level.

8. (Twice Amended) The method of manufacturing a semiconductor device as defined in claim 7,

wherein the processing [securing at least a part of a back] step is specified to be carried out by at least one technique selected from a group consisting of scraping by means of dicing, sand blast, and sandpaper and treatment by means of laser beam projection.

9. (Twice Amended) The method of manufacturing a semiconductor device as defined in claim 7, wherein the processing [securing] step results in the semiconductor element having a thickness of 50 μm or less where the semiconductor element is processed [secured].

22. (Amended) A method of manufacturing a semiconductor device, comprising: [,]

securing a semiconductor element having an integrated circuit to a board so as to be level with the board,

[securing] subjecting at least a part of a back of the semiconductor element to processing [the board so as to develop a stress level that reacts when the semiconductor element is detached from the board], wherein the processing applies a stress to the semiconductor element causing at least a part of the semiconductor element to deform when removed from the board,

wherein the [securing] subjecting at least a part of a back to processing is specified to be carried out by at least one technique selected from a group consisting of scraping by means of dicing, sand blast, and sandpaper and treatment by means of laser beam projection.